(3)

PATENT
TESSERA 3.0-078 DIV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of
Fjelstad et al.

Application No. 09/020,647

Filed: February 9, 1998

For: Semiconductor Chip Package
With Fan-In Leads

Group Art Unit: 2814

Examiner: D. Graybill

Date: May 15, 2001

Commissioner for Patents
Washington, D.C. 20231

APPEAL BRIEF UNDER 37 C.F.R. § 1.192(a)

Sir:

This Appeal Brief is filed pursuant to an appeal from the decision of the Primary Examiner finally rejecting the pending claims in the above-identified patent application. A petition requesting a one-month extension of time in which to file the Appeal Brief originally due May 12, 2001 is filed herewith. The Commissioner is hereby authorized to charge $110.00 for the one-month extension petition and the $310.00 fee for filing the Appeal Brief required by 37 C.F.R 1.17(c), and any other fees that may be due in connection with this Appeal Brief to Deposit Account No. 12-1095.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231 on May 15, 2001.

Michael J. Doherty
(Signature)

MICHAEL J. DOHERTY
Typed or Printed Name of Person Signing Certificate

I. REAL PARTY IN INTEREST

The real party in interest in this case is Tessera, Inc., a corporation of Delaware, having a place of business at 3099 Orchard Drive, San Jose, California 95134.

II. RELATED APPEALS AND INTERFERENCES

No related appeals or interferences are known to Appellants, Appellants' attorneys or the assignee, Tessera, Inc., which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-11, 21-23 and 25-34 are pending in the present application. Claims 12-20 have been cancelled and claim 24 has been withdrawn from consideration. Claims 1-11, 21-23 and 25-34 are rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection mailed November 9, 2000.

V. SUMMARY OF THE INVENTION

The present invention relates to methods of making semiconductor chip packages including a semiconductor chip and a compliant layer. The invention recited in claim 1 and the other claims of the present application relates to methods of

selectively forming elongated, flexible bond ribbons over a compliant layer, whereby the elongated bond ribbons extend along sloping edges of the compliant layer. Referring to Applicants' FIGS. 1A-1E and 2, a semiconductor chip 100 has a central region 115 bounded by contacts 110 on a contact-bearing face 120 of chip 100. The contact-bearing face 120 of the chip is covered by a passivation layer 130 having apertures for exposing the chip contacts 110. Referring to FIG. 1C, a compliant layer 140 having a substantially flat top surface is formed atop passivation layer 130. The compliant layer 140 is located over the central region 115 of semiconductor chip 100 and is surrounded by the chip contacts 110. The compliant layer is formed such that it has a substantially flat top surface 147 and edges that gradually slope down to the top surface of the dielectric passivation layer 130. The sloping edges preferably have a first transition region near the top surface of the compliant layer and a second transition region near the bottom surface of the compliant layer so that both the first transition region and the second transition region have a radius of curvature. Specification at page 5, lines 3-11.

Referring to FIG. 1D, a plating seed layer 150 is deposited atop selected portions of compliant layer 140. Referring to FIG. 1E, a photoresist 160 is applied to the exposed surfaces of the assembly and the photoresist is then exposed and developed. Elongated bond ribbons 170 are then selectively electroplated atop both the first dielectric protective layer and the compliant layer, whereby each bond ribbon electrically connects each chip contact 110 to a respective terminal 175 positioned atop the compliant layer.

See Specification at page 11, lines 17-20. FIG. 2 shows a perspective view of the elongated bond ribbons extending between the chip contacts 110 and terminals 175. As clearly shown in FIG. 2, the elongated bond ribbons 170 extend along the sloping edge surfaces 145 of compliant layer 140. As noted above, the compliant layer has sloped peripheral edges so that the overlying bond ribbons are curved rather than kinked.

VII. ISSUES

Whether claims 1-4, 6-7, 11, 21-23, 25-30 and 33-34 are unpatentable under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 5,070,297 to *Kwon et al.* ("*Kwon*") or, in the alternative, under 35 U.S.C. § 103(a) as obvious over *Kwon*.

Whether claims 9-10 and 31-32 are unpatentable under 35 U.S.C. § 103(a) over *Kwon* and further in view of U.S. Patent 5,874,782 to *Palagonia* ("*Palagonia*").

VIII. GROUPING OF CLAIMS

Claims 1-11, 21-23 and 25-34 do not stand or fall together. Thus, the arguments presented below are directed to the following two groups of claims:

1. Claims 1-4, 6-7, 11, 21-23, 25-30 and 33-34.
2. Claims 9-10 and 31-32.

IX. ARGUMENT

1. Claims 1-4, 6-7, 11, 21-23, 25-30 and 33-34.

The Examiner rejected claims 1-4, 6-7, 11, 21-23, 25-30 and 33-34 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,070,297 to *Kwon et al.*, and in the alternative, under 35 U.S.C. § 103(a) as obvious over *Kwon*. Referring to FIGS. 4A-4H thereof, *Kwon* discloses a method of making integrated circuit testing devices including providing a layer of a compliant material 32 atop a silicone dioxide layer 34, with active element 36 disposed between silicone substrate 38 and silicone dioxide layer 34. Referring to FIG 4B, vias are formed in compliant layers 32 to expose portions of the active element 36. Each via forms a conical-shaped opening extending between the top and bottom surfaces of compliant layer 32. Metal contact layer 28 and conductive coating 30 are then deposited within the via openings in compliant material 32, as shown in FIG. 4C. Referring to FIG. 4D, a compliant protective coating 26 is formed atop compliant material 32, metal contact layer 28 and conductive coating 30. The compliant protective coating 26 is etched to form openings extending to metal contact layer 28, and a seed layer is sputtered over the protective coating layer 26 to form a connector base in each opening in the protective coating 26. A conductive metal layer is then sputtered over connector base 24 to form connector caps 22. Referring to FIG. 4H, test probes 16 are attached to the assembly and electrically

interconnected with the conductive metal 28, 30 in the vias. Thus, *Kwon* teaches forming metallized vias by first forming via openings in a compliant layer and then depositing one or more layers of conductive material in the via openings.

Claim 1 is unanticipated by and unobvious over *Kwon* because the reference neither discloses nor suggests the step of "selectively electroplating elongated bond ribbons atop the first dielectric protective layer and the compliant layer . . . wherein said elongated bond ribbons extend along the sloping edges of said compliant layer." The conductive metal layers 28 and 30 deposited over *Kwon's* via openings do not form "elongated bond ribbons." Rather, *Kwon*'s metallized vias have a V or conical-shaped cross-section that teaches away from Applicants' claimed "elongated bond ribbons." In addition, a top plan view of *Kwon*'s metallized vias, similar to the view shown in FIG. 1 thereof, would show metal layers 28 and 30 to be circular. This "circular" structure clearly doesn't teach or suggest Applicants' step of "selectively electroplating elongated bond ribbons." Moreover, *Kwon* provides no teaching or suggestion to form the elongated bond ribbons "along the sloping edge surfaces of said compliant layer." In sum, there is nothing "elongated" about *Kwon*'s metallized vias. For all of these reasons, claim 1 is unanticipated by and unobvious over *Kwon* and is otherwise allowable. Claims 2-4 are also unanticipated and unobvious by virtue of their dependence from claim 1, which is unanticipated and unobvious for the reasons set forth above. Claim 6 is unanticipated and unobvious by

virtue of its dependence from claim 4, and claim 7 is unanticipated and unobvious by virtue of its dependence from claim 1.

The limitations recited in claim 11 are shown in FIG. 1C of the present application and are described in the specification at, *inter alia*, page 7, lines 5-6. Referring to FIG. 1C of the present application, compliant layer 140 has a top surface 147, a bottom surface and peripheral edges 145 that slope between the top and bottom surfaces. The sloped peripheral edges provide increased reliability for the bond ribbons formed thereon because the bond ribbons formed thereon are curved rather than kinked. Specification at page 7, lines 5-6. This particular limitation is neither disclosed nor suggested by *Kwon* which shows (FIG. 4B) that the vias have sidewalls that form angles with the top and bottom surfaces of compliant layer 32. When *Kwon* deposits metal layers 28, 30, these layers take the shape of the underlying via opening. Thus, the metal layers 28, 30 also have distinct angles at the top and bottom of the vias, thereby minimizing the reliability of *Kwon*'s conductive layer at these points. Thus, claim 11 is also unanticipated and unobvious over *Kwon* because *Kwon* neither discloses nor suggests a compliant layer having sloping edges with "a first transition region near the top surface of the compliant layer and a second transition region near the bottom surface of the compliant layer and <u>wherein both the first transition region and the second transition region have a radius of curvature</u>." (Emphasis added) Claim

11 is also unanticipated and unobvious by virtue of its dependence from claim 1, which is allowable for the reasons set forth above.

Amended claim 21 is unanticipated and unobvious over *Kwon* because the cited reference neither discloses nor suggests the step of "selectively forming elongated, flexible bond ribbons over said compliant layer." As noted above, Applicants' bond ribbons 170, shown in FIG. 2 of the present application, are elongated and extend along the one or more sloping edge surfaces of the compliant layer. This particular limitation is neither disclosed nor suggested by *Kwon* which teaches providing conductive metal layers 28 and 30 in via openings of a compliant material 32 to form metallized vias. For all of these reasons, claim 21 is unanticipated by and unobvious over *Kwon* and is otherwise allowable. Claims 22 and 23 are also unanticipated by and unobvious over *Kwon* by virtue of their dependence from claim 21, which is unanticipated and unobvious for the reasons set forth above. Claims 25-30 and 33 are also unanticipated and unobvious by virtue of their dependence, either directly or indirectly, from claim 21, which is allowable for the reasons set forth above.

Claim 34 is similar in scope to pending claim 11. Claim 34 is unanticipated by and unobvious over *Kwon* because the cited reference neither discloses nor suggests a compliant layer having sloping edge surfaces with "first transition regions near the top surface of the compliant layer and second transition regions near the bottom surface of the compliant

layer, and wherein both the first and second transition regions have respective radii of curvature." As asserted above, *Kwon's* via openings include sidewalls that form sharp angles or edges with the top and bottom surfaces of compliant layer 32. Thus, *Kwon's* via sidewalls do not have transition regions with "radii of curvature." For all of these reasons, claim 34 is unanticipated by and unobvious over *Kwon* and is otherwise allowable. Claim 34 is also allowable by virtue of its dependence from claim 33, which is unanticipated by and unobvious for the reasons set forth above.

The Examiner also rejected claims 5 and 8 under 35 U.S.C. § 103(a) as being unpatentable over *Kwon*. In response, Applicants assert that claims 5 and 8 are unobvious by virtue of their dependence, either directly or indirectly, from claim 1, which is unobvious over *Kwon* for the reasons set forth above.

2. Claims 9-10 and 31-32.

The Examiner rejected claims 9, 10, 31 and 32 under 35 U.S.C. § 103(a) as being unpatentable over *Kwon*, and further in view of U.S. Patent 5,874,782 to *Palagonia*, which discloses a wafer having elevated contact structures. Referring to FIGS. 3A and 5 thereof, *Palagonia* teaches a method including a step of dicing and separating a plurality of adjacent compliant semiconductor chip packages 22 arranged in an array on a wafer 20 following the step of forming bond ribbons 26. *Palagonia*, however, does not overcome the deficiencies of *Kwon*. Thus, claims 9 and 10 are unobvious

over the combination of *Kwon* and *Palagonia* and are otherwise allowable. Claims 9 and 10 are also unobvious by virtue of their dependence from claim 1, which is unobvious for the reasons set forth above. Claims 31 and 32 are unobvious over the combination of *Kwon* and *Palagonia* because the combination neither discloses nor suggests the limitations recited in the subject claims, and by virtue of their dependence from claim 21, which is unobvious for the reasons set forth above.

VIII. CONCLUSION

For the reasons set forth above, this Honorable Board should reverse the rejection as to all claims on appeal.

Respectfully submitted,

LERNER, DAVID, LITTENBERG,
KRUMHOLZ & MENTLIK, LLP

MICHAEL J. DOHERTY
Reg. No. 40,592

600 South Avenue West
Westfield, NJ 07090-1497
Tel: (908) 654-5000
Fax: (908) 654-7866

APPENDIX

A copy of the claims on appeal is set forth below.

1. A method of creating a compliant semiconductor chip package assembly comprising the steps of:

providing a first dielectric protective layer on a contact bearing surface of a semiconductor chip, wherein the semiconductor chip has a central region bounded by chip contacts of the semiconductor chip and wherein the dielectric protective layer has a plurality of apertures such that the chip contacts are exposed;

providing a compliant layer atop the first dielectric protective layer within the central region, wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to the first dielectric protective layer and sloping edges between the top surface and the bottom surface; and

selectively electroplating elongated bond ribbons atop the first dielectric protective layer and the compliant layer wherein each bond ribbon electrically connects each chip contact to a respective conductive terminal on the top surface of the compliant layer, and wherein said elongated bond ribbons extend along the sloping edges of said compliant layer.

2. The method according to Claim 1 further including the step of providing a second dielectric protective layer atop exposed assembly elements on the terminal side of the assembly after the step of selectively electroplating the bond

ribbons, wherein the second dielectric protective layer has a plurality of apertures such that the terminals are exposed.

3. The method according to Claim 1 wherein the compliant layer material is selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof.

4. The method according to Claim 1 further including the step of providing for an encapsulant layer atop an exposed surface of the bond ribbons.

5. The method according to Claim 4 wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel.

6. The method according to Claim 4 further including the step of providing for a second dielectric protective layer atop the encapsulant layer wherein the second dielectric protective layer has a plurality of apertures such that terminal positions are exposed.

7. The method according to Claim 1 wherein a silicon dioxide passivation layer on the face surface of the semiconductor chip comprises the first dielectric protective layer.

8. The method according to Claim 1 further including the step of plating a barrier metal atop the semiconductor chip contacts, prior to the step of providing the compliant layer, whereby the barrier metal helps to prevent voiding at the boundary between the semiconductor chip contacts and the bond ribbons.

9. The method according to Claim 1 applied simultaneously to a multiplicity of undiced semiconductor chips on a wafer to form a corresponding multiplicity of compliant semiconductor chip packages, the method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

10. The method according to Claim 1 applied simultaneously to a multiplicity of adjacent semiconductor chips arranged in an array to form a corresponding multiplicity of compliant semiconductor chip packages, the method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

11. The method according to Claim 1 wherein the sloping edges of the compliant layer have a first transition region near the top surface of the compliant layer and a second transition region near the bottom surface of the compliant layer and wherein both the first transition region and the second transition region have a radius of curvature.

21. A method of making a compliant microelectronic assembly comprising the steps of:

providing a microelectronic element having a first surface and a plurality of contacts disposed on the first surface thereof;

providing a compliant layer over the first surface of said microelectronic element, said compliant layer having a bottom surface facing toward said first surface of

said microelectronic element, a top surface facing upwardly away from said microelectronic element and one or more edge surfaces extending between said top and bottom surfaces, and then

selectively forming elongated, flexible bond ribbons over said compliant layer so that said bond ribbons extend over said top surface and one or more of said edge surfaces and said bond ribbons electrically connect said contacts to conductive terminals overlying the top surface of said compliant layer.

22. The method as claimed in claim 21, wherein said contacts on said microelectronic element are disposed in a first region of said first surface, said compliant layer overlies a second region of said first surface, and one or more edge surfaces include one or more border edge surfaces extending along one or more borders between said first and second regions.

23. The method as claimed in claim 21, wherein said selectively forming bond ribbons step includes selectively electroplating said bond ribbons.

24. The method as claimed in claim 21, wherein said selectively forming bond ribbons step includes electrolessly plating a conductive material over the top of said assembly and selectively etching away said conductive material.

25. The method as claimed in claim 21, further comprising the step of:

before the providing a compliant layer step, providing a first dielectric protective layer on the first surface of the microelectronic element, the first dielectric layer having a plurality of apertures therein so that said contacts are accessible therethrough, the providing the compliant layer step including the step of providing the compliant layer over said first dielectric protective layer.

26. The method as claimed in claim 25, the selectively forming flexible bond ribbons step including selectively electroplating said bond ribbons atop said first dielectric protective layer and said compliant layer.

27. The method as claimed in claim 21, further including the step of providing a dielectric cover layer over said compliant layer and said bond ribbons after the step of selectively forming the bond ribbons, wherein the cover layer has a plurality of apertures so that said terminals are accessible therethrough.

28. The method as claimed in claim 21, further including the step of providing an encapsulant layer over an exposed surface of the bond ribbons.

29. The method as claimed in claim 28, further including the step of providing a second dielectric protective layer atop the encapsulant layer wherein the second dielectric protective layer has a plurality of apertures so that said terminals are accessible therethrough.

30. The method as claimed in claim 21, further including the step of depositing a barrier metal atop said contacts,

prior to the step of forming the bond ribbons, whereby the barrier metal helps to prevent voiding between the contacts and the bond ribbons.

31. The method as claimed in claim 21, the method being applied to a plurality of undiced semiconductor chips on a wafer to form a corresponding plurality of compliant semiconductor chip packages, the method further including the step of separating the packages following the step of depositing the bond ribbons.

32. The method as claimed in claim 21, the method being applied to a plurality of adjacent semiconductor chips arranged in an array to form a corresponding multiplicity of compliant semiconductor chip packages, the method further including the step of separating the packages following the step for selectively electroplating the bond ribbons.

33. The method as claimed in claim 21, wherein the edge surfaces of the compliant layer are sloping surfaces which extend in both vertical and horizontal directions.

34. The method as claimed in claim 33, wherein at least some of said sloping edge surfaces have first transition regions near the top surface of the compliant layer and second transition regions near the bottom surface of the compliant layer, and wherein both the first and second transition regions have respective radii of curvature.